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Prior Art
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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject: Serial No. 09/160,965 09/25/98

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A NOVEL PLANARIZATION METHOD OF COPPER DAMASCENE

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 4,789,648 to Chow et al, "Method For Producing Coplanar Multi-Level Metal/Insulator Films On A Substrate And For Forming Patterned Conductive Lines Simultaneously With Stud Vias", shows a method for forming metal interconnects that use CMP of metal (W or Al) alloys.

U.S. Patent 4,702,792 to Chow et al, "Method Of Forming Fine Conductive Lines, Patterns And Connectors", discloses a method for producing coplanar multi-level metal/insulator films on a substrate and for forming patterned conductive lines simultaneously with stud vias.

U.S. Patent 5,693,563 to Teong, "Etch Stop For Copper Damascene Process", shows a method of forming an etch stop for a copper damascene process with CMP.

U.S. Patent 4,954,459 to Avanzino et al, "Method Of Planarization Of Topologies In Integrated Circuit Structures", shows a planarization technique using a reverse mask and etch back only technique.

U.S. Patent 5,567,300 to Datta et al, "Electrochemical, Metal Removal Technique For Planarizatin Of Surfaces", describes a high speed electrochemical metal removal technique for planarization of multilayer copper interconnections in thin film modules.

U.S. Patent 5,346,584 to Nasr et al, "Planarization Process For IC Trench Isolation Using Oxidized Polysilicon Filler", discloses a shallow trench isolation planarization method using an etch back process with a reverse tone filler mask and an oxide filler in the depressions above the trenches and CMP process.

U.S. Patent 5,494,857 to Cooperman et al, "Chemical Mechanical Planarization Of Shallow Trenches In Semiconductor Substrates", presents a shallow trench isolation planarization method using an etch back process with a reverse tone filler mask and an oxide block in the depressions above the trenches and CMP process.

U.S. Patent 5,602,423 to Jain, "Damascene Conductors With Embedded Pillars", shows a damascene process using CMP and electroplating which uses an embedded pillar to prevent damage (e.g.) dishing, smearing, overetching).

C.Y. Chang et al, "ULSI Technology", The McGraw-Hill Companies, Inc, p.446-447, discusses damascene and dual damascene techniques.

Sincerely,

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